REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claim Rejections - 35 USC §102

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. US Re38, 456 E. Applicants respectfully traverse these rejections.

To anticipate a claim, the reference must teach each and every element of the claim. *See* MPEP §2131. As to claim 1, Patel et al. does not teach each and every element of claim 1.

Regarding claim 1, the Examiner has stated that Patel et al. teaches "detecting the narrowband interference (see col.8, lines 53-60 and col.21, lines 38-45)" Applicants respectfully point to the Examiner that a careful reading of the cited section reveal that Patel et al. actually describes synchronizing a controlled oscillator by developing an automatic-frequency-and-phase-control (AFPC) signal. The AFPC signal is developed by applying a non-liner procedure to produce second harmonics, which is then used to regenerate the baud frequency. The baud frequency is used to determine the error of the controlled oscillator (*see* col. 8, lines 53-60). Further, in col. 21, lines 38-45, Patel et al. actually describes the internal structure with reference to figure 4 of a clock generator 23 shown in Figure 1. In the cited sections, Patel et al. describes the circuit that regenerates baud frequency for symbol timing from symbol code. Nowhere in the cited section, Patel et al. describes detecting narrowband interference in the transmission as recited in claim 1.

Further, the Examiner has stated that Patel et al. teaches "**backtracking** over **previously decoded portions** of the transmission (see fig.2 element **training signal** or loop-back)" (emphasis in original and added). A careful reading of the cited sections reveals that Patel et al. does not even discuss backtracking over previously decoded portion. In fact, the training signal is actually provided periodically to adjust the weighted coefficients of multiple-tap digital filter

in the equalizer 36. The training signal is contained in the initial data segment of each data field. The microprocessor compares the received training signal with a known training sequence and determines weighted coefficients accordingly (*see* col. 13, lines 38-64). Thus, Patel et al. does not describe backtracking over previously decoded portions of the transmission as recited in claim 1. Accordingly, Patel et al. does not teach each and every element of the claim as required to anticipate claim 1 and therefore, claim 1 is patentably distinguishable from Patel et al.

Claims 2-14 depend from claim 1 and are patentably distinguishable from Patel et al. for at least the same reasons as claim 1.

Further, the Examiner has rejected claims 2-14 as being inherently included in Patel et al. without providing any explanation as to the relevance of inherency of recited steps in the disclosure of Patel et al. "To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *See* M.P.E.P. §2163.07(a). As explained above, Patel et al. does not even teach all limitations of claim 1 therefore, the limitations recited in claims 2-14 cannot be inherently present in Patel et al. Accordingly, claims 2-14 are further patentably distinguishable from Patel et al.

Claim Rejections - 35 USC §102

Claims 15-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Agazzi et al U.S. Pub no 2001/0035994. Applicants respectfully traverse these rejections.

As to claims 15 and 22, the Examiner has stated that Agazzi et al. teaches:

> "a first control and information line coupled to the digital processing unit, the first control and information (see fig.5 **element 96 Fc**) line providing configuration and operational information of the digital processing unit ... and a second control and information line (see fig.5 **element fc** and page 4, paragraph [0064]) coupled to the sequential decoder, the second control and information line providing configuration and

operational information of the sequential decoder."
(Emphasis added)

Applicants respectfully point to the Examiner that a careful reading of cited section and figures reveal that the element Fc is actually a clock signal generated by the timing recovery unit 96. Even the cited section very clearly states that Fc is Fb/16 = 312.5 MHz (*see* paragraph 0064). In contrast, claims 15 and 22 recite information lines providing configuration and operational information regarding respective units. Agazzi et al. does not teach this limitation and therefore does not anticipate claims 15 and 22.. Accordingly, claims 15 and 22 are clearly distinguishable from Agazzi et al.

Claims 16-21 depend from claim 15 and are patentably distinguishable from Agazzi et al. for at least the same reasons as claim 15. Further, the Examiner has rejected claims 16-17, and 19-21 as being "inherently" taught by Agazzi et al. without providing any relevance of the teachings of Agazzi et al. with the limitations recited in these claims. For example, as to claim as to claim 16, the Examiner has assumed that Agazzi et al. inherently includes an interference detection unit without providing any reference to interference detection function in Agazzi et al. Similarly, the relevance of Agazzi et al.'s teaching related to the limitations of claims 19-21 is also not provided by the Examiner. Accordingly, Applicants believe that these claims are further patentably distinguishable from Agazzi et al.

New claims 23-26 have been added. These claims recite a communication device with a decoder configured to backtrack through the symbols for state transitions. As explained above, neither of the cited references teach, suggest, or describe backtracking as recited in these claims. Accordingly, Applicants believe that these claims are patentably distinguishable from the cited references.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

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